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REPORT PP-T-9672-1

UNITED STATES ARMY

FRANKFORD ARSENAL

THE PROCESSES AND DEVELOPMENT OF TECHNIQUES OF
MINIATURIZED GOLD PLATED THROUGH HOLES
IN PRINTED CIRCUITS

by

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MAY 1963

PHILADELPHIA 37, PA.

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FRANKFORD ARSENAL
PHILADELPHIA 37, PENNSYLVANIA

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THE PROCESSES AND DEVELOPMENT OF TECHNIQUES OF MINIATURIZED GOLD PLATED THROUGH HOLES IN PRINTED CIRCUITS

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ABSTRACT

This report describes the techniques developed and the procedures used successfully copper, nickel and gold plating small (0.040", 0.031", 0.020" and 0.016") diameter plated through holes utilized as interface (side-to-side) connections in double sided printed circuit boards.

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Section Title

INTRODUCTION

In the initial stages of printed circuit manufacturing only one side of the insulator had a conductive pattern. These single sided boards were basic and presented no great difficulty in fabrication but because of geometric and space considerations they were limited in military application. It thus became necessary in the evolutionary chain to utilize both sides of the insulated board for a conductive pattern. This resulted in a printed circuit board that had copper foil on both sides.

Initially, eyelets were used to make the interface (side-to-side) connections on the double sided circuit boards because of their ready accessibility and theorized ability to make positive mechanical contact between the copper conductive patterns. This technique was deemed adequate for the initial double sided circuit boards produced, but fabrication costs increased rapidly and a tendency toward weakening of the structural characteristics of the board itself was noted as circuit configurations became much more complex and the number of holes for side-to-side connections increased in conjunction with pattern complexity.

As with all militarily applicable components, the circuit board was subject to stringent environmental tests. As a result of these tests, a controversy arose as to the eyelet's ability, to successfully expand and contract at the same rate as the conductive pattern. This controversy accelerated the development of sophisticated plating processes which emphasized chemical reduction techniques as a means of depositing a metallic film on plastic.

Initially, metal plating was not stressed in double sided circuit board fabrication because of the problems encountered in metal to plastic deposition. The standard electrolytic copper baths were not acceptable because they could not deposit an adhering metal coat upon the plastic insulator. These electrolytic baths lacked the necessary activating and reducing agents to insure metal adhesion within the interface connecting holes. The problem was solved by the development of techniques which chemically activated the plastic to receive an adhering metallic film on the nonconductive substrate. The activating technique consisted of utilizing a chemical reducing (electroless) process for depositing a very thin layer of conductive copper to prepare the interface connections for the subsequent electrolytic copper plating. This electroless process made the side-to-side connections conductive for subsequent plating operations.

To accommodate standard component leads the .052 inch drilled hole was utilized as the interface connection in developing the initial chemical reduction process for double sided printed circuit boards. With the advent of semiconductor devices (transistors, diodes, rectifiers, etc.) and microminiaturization techniques applicable to military circuit boards it became evident that much smaller side-to-side connections would be required and these connections in turn required the establishment of refined methods for making the small (.040", .031", .020", and .016") diameter through holes.

In conjunction with the smaller through hole plating techniques, metals other then copper were being requisitioned for military requirements for double sided circuit boards. Nickel and gold were required to give greater film hardness, etch resistance, electrical conductivity, solderability, non-galling of mating contacts, wear and corrosion resistance.

PROCEDURE

The program was conveniently divided into four experiments, one for each size hole. The procedure for each test was identical except for the plating times which were varied. Sixty glass epoxy (G10) printed circuit boards, copper laminated on both sides, size 3" x 2½", were cut to size and ten holes were accurately drilled in each board according to the engineering design with the aid of a master template which contained the circuit pattern. The holes were carefully deburred by hand using fine emery cloth. These holes when plated connected the two copper foils. All the plating and accessory baths were made up and brought to operating conditions (See Figure 1, and Charts 1, 3, 5, and 7). It should be emphasized at this point that the plating baths used in the through hole process must be carefully prepared following the make up instructions completely. This is particularly true in preparing the electroless copper and electroless nickel baths. In the electrolytic copper and electrolytic gold plating baths the geometry of the setup is critical and depends upon the design of the circuit being plated. The entire plating process must be rigidly controlled. This rigid control is necessary because variation in the plating thickness could prevent optimum component insertion. With this rigid control, the plating thickness will be duplicated from circuit to circuit.

From the initial to the final step in the boards fabrication process, cleanliness was immensely important. The cut and drilled double sided copper boards were thoroughly scrubbed by hand using a scrub cleaner and were rinsed in running tap water to insure removal of any residue from the laminating process or subsequent handling. It must be noted that it is very important that the copper circuit side of the board be free from fingerprints, oils, or other agents that may reduce the adhesion of the plated coat. This is particularly true in the drilled hole where any contamination may make it difficult to bond the electroless copper to the hole walls. An indication that the copper laminated surface has been properly cleaned is its ability to maintain an unbroken film of water over the entire cleaned surface.

The scrub cleaning operation was followed by depositing electroless copper on the plastic hole walls (See Chart 2 and Figure 2). All of the boards regardless of hole size were immersed in the electroless copper bath for a period of twenty-five (25) minutes. This immersion period theoretically gave a build-up of approximately .000020 inches.

The electroless deposition was immediately followed by a electrolytic copper plating process (See Chart 4 and Figure 3) to increase the thickness and strengthen the electroless copper deposit in the holes. For plating thickness and time (See Chart 9). The copper plated board was then air dried and the holes were visually inspected to detect any obvious defects.

The electroless nickel process was applied to the board (See Chart 6). Each board was immersed in the nickel solution for twenty-five (25) minutes which theoretically gave a build-up of approximately 0.0002 inches. The nickel process is followed by the application of the circuit pattern by the utilization of the silk screen method (See Figure 4). The plated board was placed under the silk screen which had the desired circuit pattern enmeshed upon it, and the black resist material (Meaker Co.) was applied by means of a squeegee and then the board was removed and placed into an oven for fifteen (15) minutes at 250°F for curing.

The silk screening procedure was followed by the electrolytic gold plating process (See Figure 5 and Chart 8). The gold plating was accomplished by using a relatively small amount of current somewhere in the nature of 70 milliamperes per square inch which theoretically yielded a plating thickness of 0.0001" for 15 minutes of plating (See Chart 10.) The black resist material was then removed by soaking the boards into a solution of trichlorethylene for approximately two minutes. The boards were rinsed and air dried and were placed in a spray etching machine where the unwanted metal was etched away with a Ferric Chloride solution in two minutes, thus leaving the gold plated circuit pattern. The ten holes in each board were then checked with an ohmmeter for continuity and recorded (See Figure 6).

From previous experience in this field a few pertinent facts had been accumulated which proved very useful in the current project. Probably the most important knowledge gained was that the initial drilling, deburring, and cleaning operations must be stringently controlled and that so-called short-cuts must be avoided. Strict attention to these initial details proved that the preparation of the surface of the circuit board was probably more important than the actual plating operations, although it is not intended here to minimize the importance of the latter processes. It was observed that the adhesion of the initial electroless copper film on the non-conductive substrate was the prime factor in producing high quality printed circuit boards. To achieve this adhesion the drilled hole must be properly deburred, otherwise the copper deposit will build-up at the sharp ragged edges and form what is commonly called treed deposits which results in very little adherence.

The objective of the work reported herein was to determine the feasibilities and the problems encountered in plating small (0.040", 0.031", 0.020" and 0.016") diameter through holes in double sided printed circuit boards utilizing copper, nickel and gold films with particular emphasis upon the minimal plating times.

RESULTS AND DISCUSSION

The results of the four tests indicate a successful approach and optimum techniques utilized in plating small diameter holes of printed circuit boards. The results substaniate knowledge gained in previous experiments using larger sized holes, namely, that the drilling, deburring, and cleaning procedures are extremely important and that any short-cuts should be avoided.

The electrolytic plating times for both copper (45 minutes) and gold (15 minutes) used on the first twenty (20) boards in Test No. 1 were chosen as the ideal plating times, therefore, they were considered to present the least amount of difficulties which the actual plating later verified. The plating times of the remaining forty (40) boards were decreased in an effort to obtain minimal requirements and the results indicated that regardless of the plating times the circuit boards were all successfully plated.

The following two tests were conducted with the same approach in mind as the first test and the results obtained were essentially the same. It was determined that the plating times of the initial twenty (20) boards in the second test should be reduced to 23 minutes for the copper plating and 8 minutes for the gold plating. These twenty (20) boards were all successfully plated; consequently, the remaining forty (40) boards were plated with a reduction in the plating time and they also were evaluated as being successful.

The results of Test No. 4 were slightly different from the results of the three previous tests. Although the first forty (40) boards were successfully plated, all of the last twenty (20) boards were not. There were two hundred (200) holes to be plated in the last twenty (20) boards and one hundred and seventy (170) holes were successfully plated which is 85 per cent of the holes, but approaching the problem from the more realistic angle, there were only twelve (12) boards of the twenty (20) which were designated satisfactory, which of course, is only 60 per cent. The results of these last twenty (20) boards are not to be considered disappointing, when one considers the plating times used; four (4) minutes for copper plating and two (2) minutes for gold plating. These short plating times would rarely if ever be used in the practical application of producing printed circuits.

CONCLUSIONS

It was determined to be feasible to gold plate through small diametered holes (0.040", 0.031", 0.020", and 0.016") of double sided printed circuit boards.

There were no problems encountered in the plating of printed circuit boards having (0.040", 0.031", and 0.020") diameter holes.

Successful gold plated through holes were and can be achieved on printed circuit boards having 0.016" holes using eight (8) and six (6) minutes copper plating times and four (4) minutes gold plating times.

Printed circuit boards with plated through holes having 0.016" diameter were successfully accomplished for sixty (60) per cent of the boards using plating times of four (4) minutes for copper and two (2) minutes gold. These plating times are unrealistic in practice and would rarely be used.

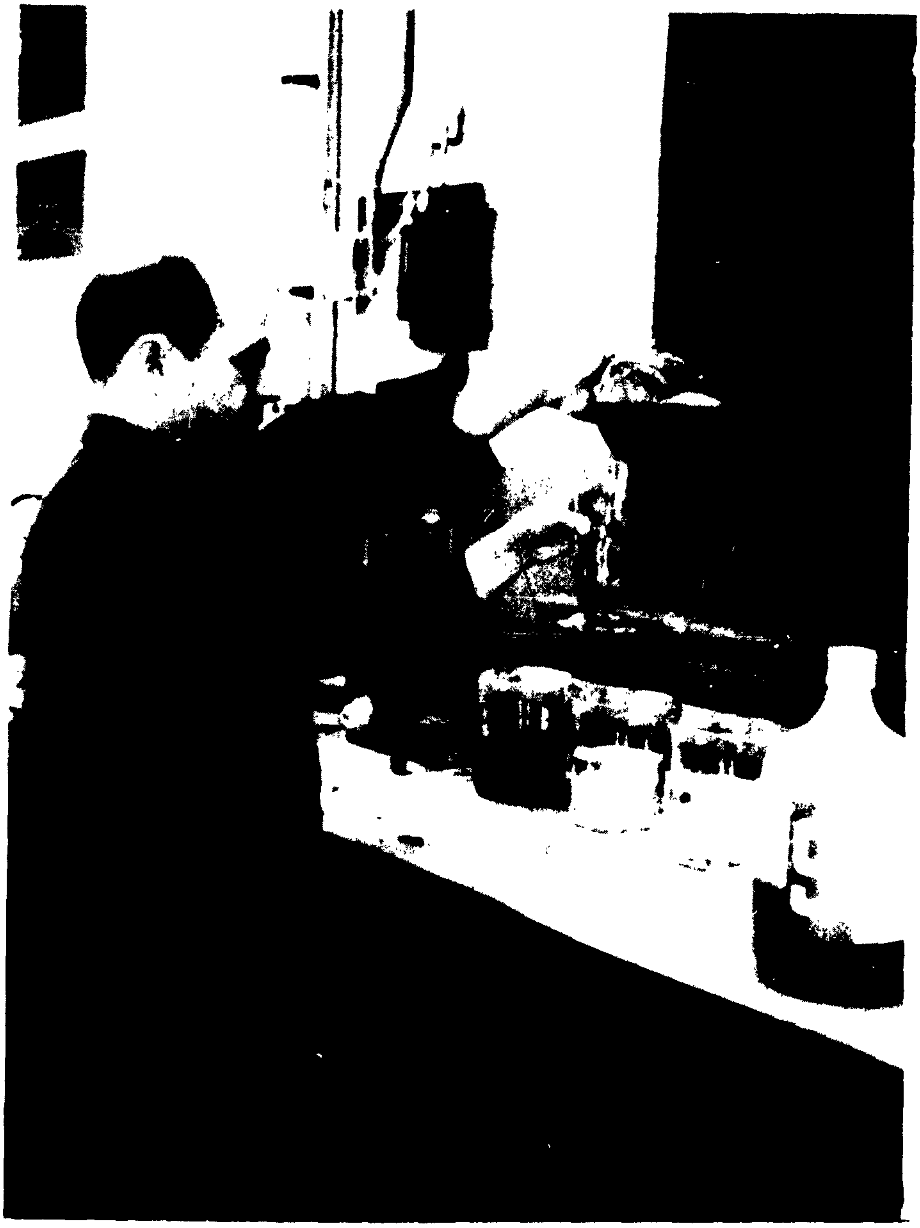

Figure 1. Making up Plating Baths

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Figure 2. Electroless Copper Plating Arrangement

76-2215 1866/ORD-63/

Figure 3. Electrolytic Copper Plating

Figure 4. Applying Circuit Pattern Using a Silk Screen

36-2715 1865/ORD-63/

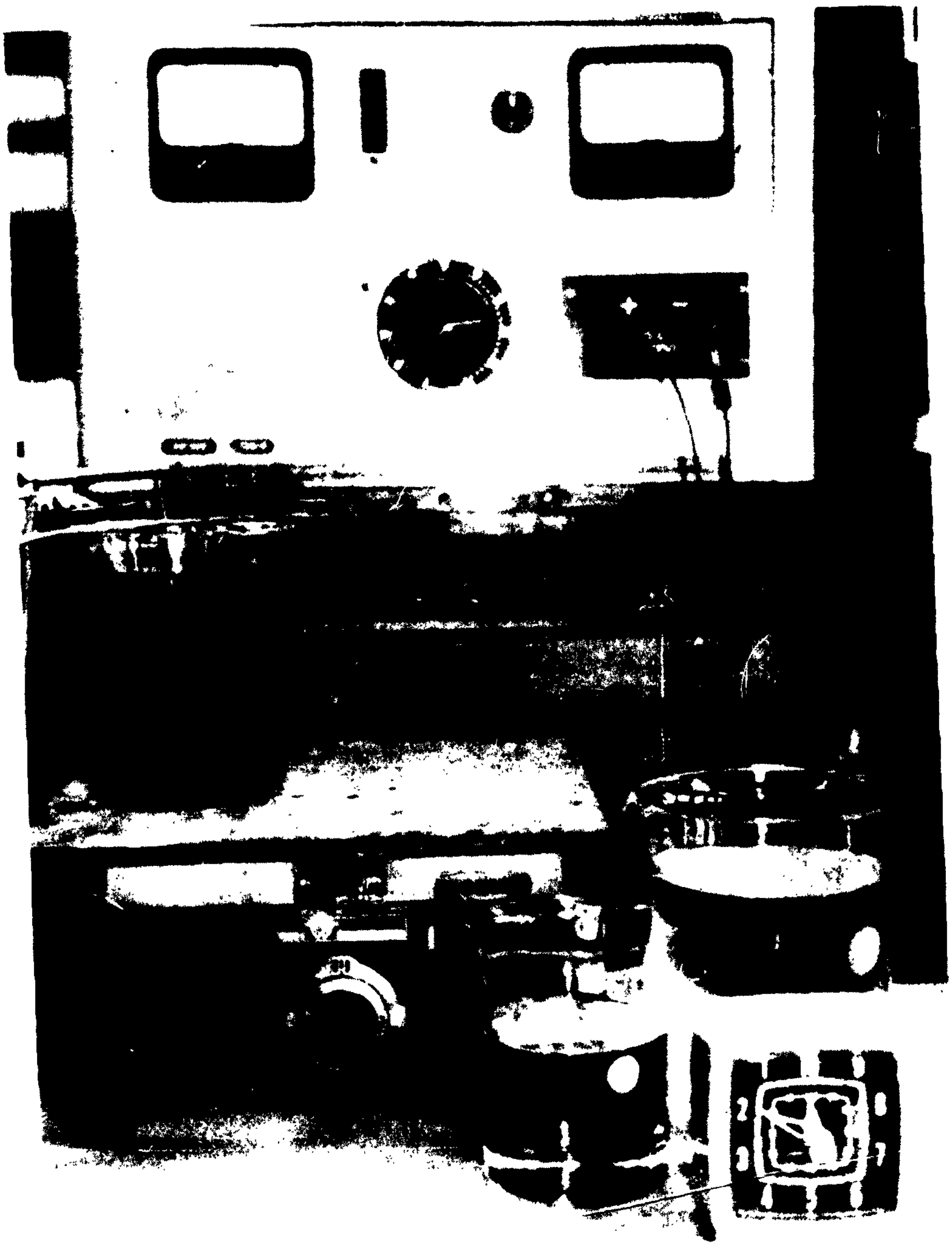

Figure 5. Gold Plating Arrangement

F-2715 1864/ORD-63/

Figure 6. Checking Boards for Continuity

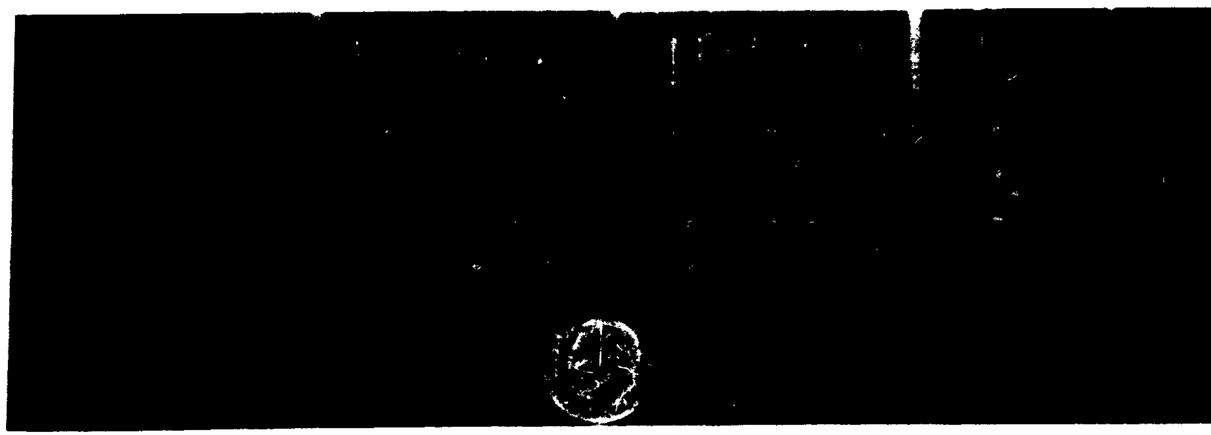

Figure 7. Printed Circuit Boards Used in Tests. Hole Sizes are, from Left to Right, 0.016", 0.020", 0.031", and 0.040" Diameter

CHART ONE

Electroless Copper Bath Make-Up
(Shipley Process)

1. Al-Chelate
   1 part concentrate, 15 parts water.

2. Cupric Chloride
   Dissolve 3/4 lb. cupric chloride in 2 gals. water, then add 1 gal.

3. Hydrochloric Acid
   33% Muriatic Acid
   Add 1 part Muriatic acid to 2 parts water.

4. Reagent H Cl
   Add 1 part reagent grade hydrochloric acid to 2 parts distilled water. (Do not use muriatic acid)

5. Catalyst 6F
   Use as supplied. Do not dilute.

6. Accelerator 6F
   1 part concentrate, 1 part water.

7. Copper Mix #3
   In diluting the copper concentrate the water temperature should be the same as the room temperature.

   65°F dilution = 1 part #3A, 5 parts water, 1 part #3B
   70°F dilution = 1 part #3A, 6 parts water, 1 part #3B

   75°F dilution = 1 part #3A, 7 parts water, 1 part #3B
   80°F dilution = 1 part #3A, 8 parts water, 1 part #3B

CHART TWO

Electroless Copper Plating Procedure

1. Scrub board clean with Shipley Scrub Cleaner #11.
2. Water Rinse.
3. Al-Chelate clean for three (3) minutes at 180°F.
4. Water Rinse.
5. Cupric Chloride immersion for three (3) minutes.
6. Water Rinse.
7. Hydrochloric acid dip for one (1) minute.
8. Water Rinse.
9. Reagent Hydrochloric acid dip for three (3) minutes.
10. Catalyst immersion for five (5) minutes.
11. Water Rinse.
12. Another Water Rinse.
13. Accelerator immersion for five (5) minutes. Can remain in this solution up to sixty minutes without any deleterious effects.
14. Water Rinse.
15. Electroless Copper Mix immersion for twenty-five (25) minutes.
16. Water Rinse.

CHART THREE

Electrolytic Copper Bath Make-Up

Solution Composition:	
Copper Sulphate	209.2 gms per liter (28 oz. per gal.)
Sulphuric Acid	52.3 gms per liter (7 oz. per gal.)
Operating Conditions:	
Temperature	72°F (Room)
Voltage	1 to 4 Volts
Current Density	175 milliamps per sq. in. (25 amps per sq. ft.)

CHART FOUR

Electrolytic Copper Plating Procedure

1. Al-Chelate clean for one (1) minute at 180°F.
2. Water Rinse.
3. Immerse in 33% Hydrochloric acid for approximately fifteen (15) seconds.
4. Water Rinse.
5. Enter Electrolytic Copper Bath with current on for immediate plating.
6. Water Rinse.
7. Air Dry.

CHART FIVE

Electroless Nickel Bath Make-Up
(Enthone Process)

1. Dilute one part of Enplate Ni-410A with 6¼ parts of distilled water by volume.

2. Adjust the PH of this solution to 4.0-4.3 (Electrometric) by adding a sodium hydroxide solution containing 0.11 to 0.23 gms./ml of C.P. sodium hydroxide.

3. Then add ½ part by volume of Enplate Ni-410B and again adjust the PH to 4.3.

Operating Conditions:

Temperature	160° - 165°F
PH	4.3
Plating Rate	0.3 - 0.4 mils/hr.

Activator Bath Make-Up
(Enthone Process)

½ pint of Activator to one gallon of water.

CHART SIX

Electroless Nickel Plating Procedure

1. Alkaline Clean for two (2) minutes at 180°F.

2. Water Rinse.

3. Hydrochloric Acid dip for one (1) minute.

4. Water Rinse.

5. Activator immersion for thirty (30) seconds.

6. Water Rinse.

7. Electroless Nickel Solution for twenty-five (25) minutes at 165°F.

8. Water Rinse.

9. Air Dry.

CHART SEVEN

Electrolytic Gold Bath Make-Up
(Sel-Rex Process)

Autronex electroplating solutions are shipped ready for use.

Operating Conditions:

Metallic Gold Content	8.2 grams/liter
Cathode Current Density	70 ma/sq. in (Up to 12 amps/sq. ft.)
PH	3.2-4.0 electro-metric
Specific Density	8.0° to 12.0° Baume
Anodes	Platinum
Temperature	110°F
Agitation	Vigorously by Air

CHART EIGHT

Electrolytic Gold Plating Procedure

1. Dip in Ammonium Persulphate (25% by weight) for approximately fifteen (15) seconds.
2. Water Rinse.
3. Dip in HCL (33% by weight) for approximately fifteen (15) seconds.
4. Water Rinse.
5. Enter electrolytic gold plating bath with current on for immediate plating.
6. Water Rinse.
7. Air Dry.

CHART NINE

ELECTROLYTIC COPPER SULFATE PLATING 174 MA/SQ. IN. (25 ASF)

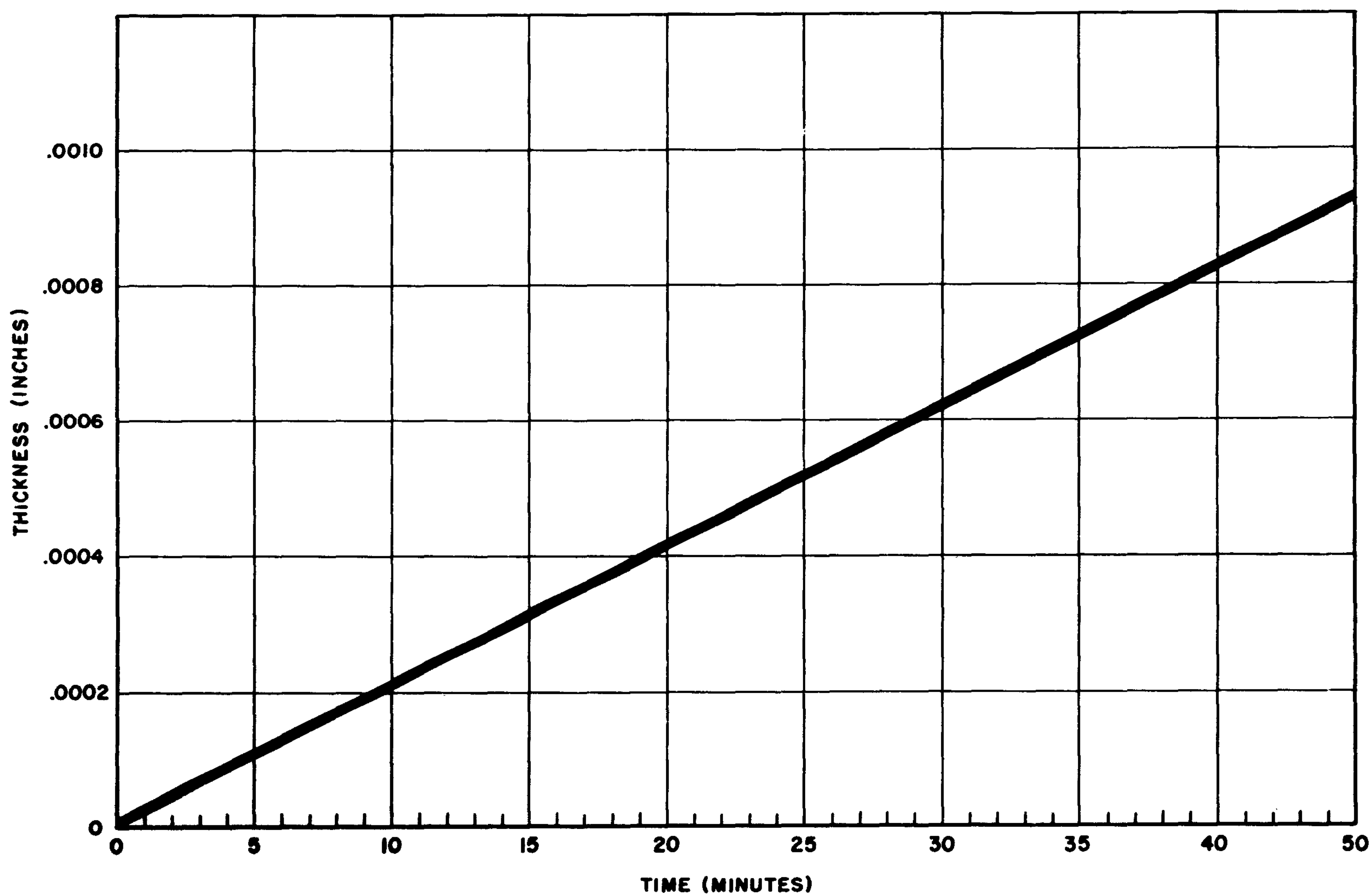

CHART TEN

ELECTROLYTIC ACID GOLD PLATING 70MA/SQ. IN. (10ASF)

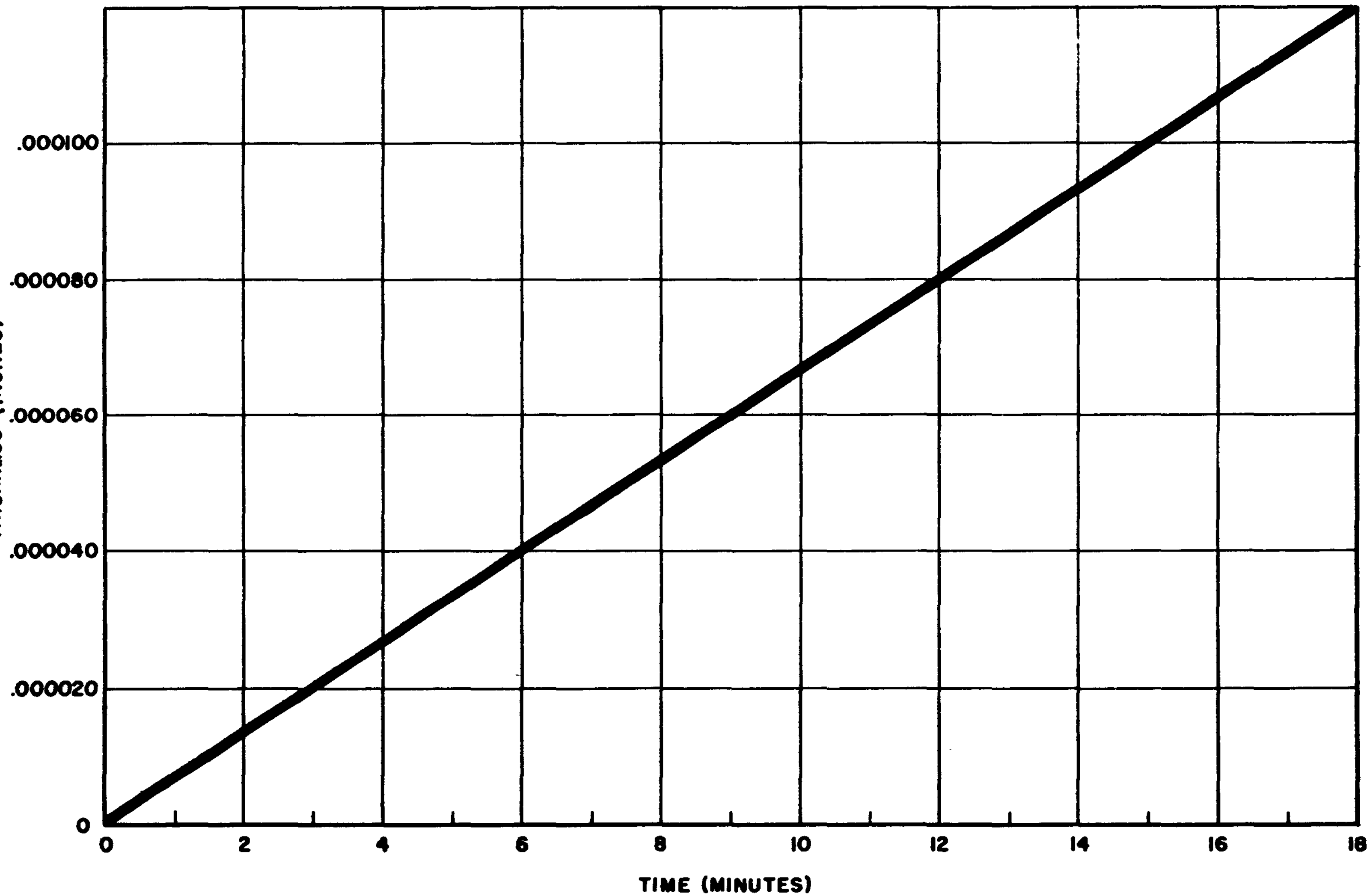

TABLE I

GOLD PLATED HOLES TEST NO. 1 (0.040" DIAMETER)

NOTE: Electroless copper plating and electroless nickel plating were each accomplished in 25 minutes.

Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)	Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)
1	45	15	Yes	31	23	8	Yes
2	45	15	Yes	32	23	8	Yes
3	45	15	Yes	33	23	8	Yes
4	45	15	Yes	34	23	8	Yes
5	45	15	Yes	35	23	8	Yes
6	45	15	Yes	36	23	8	Yes
7	45	15	Yes	37	23	8	Yes
8	45	15	Yes	38	23	8	Yes
9	45	15	Yes	39	23	8	Yes
10	45	15	Yes	40	23	8	Yes
11	45	15	Yes				
12	45	15	Yes	41	12	6	Yes
13	45	15	Yes	42	12	6	Yes
14	45	15	Yes	43	12	6	Yes
15	45	15	Yes	44	12	6	Yes
16	45	15	Yes	45	12	6	Yes
17	45	15	Yes	46	12	6	Yes
18	45	15	Yes	47	12	6	Yes
19	45	15	Yes	48	12	6	Yes
20	45	15	Yes	49	12	6	Yes
				50	12	6	Yes
21	23	8	Yes	51	12	6	Yes
22	23	8	Yes	52	12	6	Yes
23	23	8	Yes	53	12	6	Yes
24	23	8	Yes	54	12	6	Yes
25	23	8	Yes	55	12	6	Yes
26	23	8	Yes	56	12	6	Yes
27	23	8	Yes	57	12	6	Yes
28	23	8	Yes	58	12	6	Yes
29	23	8	Yes	59	12	6	Yes
30	23	8	Yes	60	12	6	Yes

TABLE II

GOLD PLATED HOLES TEST NO. 2 (0.031" DIAMETER)

NOTE: Electroless copper plating and electroless nickel plating were each accomplished in 25 minutes.

Board No.	Electro-lytic Copper Plating Time (min.)	Electro-lytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)	Board No.	Electro-lytic Copper Plating Time (min.)	Electro-lytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)
1	23	8	Yes	31	12	6	Yes
2	23	8	Yes	32	12	6	Yes
3	23	8	Yes	33	12	6	Yes
4	23	8	Yes	34	12	6	Yes
5	23	8	Yes	35	12	6	Yes
6	23	8	Yes	36	12	6	Yes
7	23	8	Yes	37	12	6	Yes
8	23	8	Yes	38	12	6	Yes
9	23	8	Yes	39	12	6	Yes
10	23	8	Yes	40	12	6	Yes
11	23	8	Yes				
12	23	8	Yes	41	8	4	Yes
13	23	8	Yes	42	8	4	Yes
14	23	8	Yes	43	8	4	Yes
15	23	8	Yes	44	8	4	Yes
16	23	8	Yes	45	8	4	Yes
17	23	8	Yes	46	8	4	Yes
18	23	8	Yes	47	8	4	Yes
19	23	8	Yes	48	8	4	Yes
20	23	8	Yes	49	8	4	Yes
				50	8	4	Yes
21	12	6	Yes	51	8	4	Yes
22	12	6	Yes	52	8	4	Yes
23	12	6	Yes	53	8	4	Yes
24	12	6	Yes	54	8	4	Yes
25	12	6	Yes	55	8	4	Yes
26	12	6	Yes	56	8	4	Yes
27	12	6	Yes	57	8	4	Yes
28	12	6	Yes	58	8	4	Yes
29	12	6	Yes	59	8	4	Yes
30	12	6	Yes	60	8	4	Yes

TABLE III

GOLD PLATED HOLES TEST NO. 3 (0.020" DIAMETER)

NOTE: Electroless copper and electroless nickel plating were each accomplished in 25 minutes.

Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)	Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)
1	12	6	Yes	31	8	4	Yes
2	12	6	Yes	32	8	4	Yes
3	12	6	Yes	33	8	4	Yes
4	12	6	Yes	34	8	4	Yes
5	12	6	Yes	35	8	4	Yes
6	12	6	Yes	36	8	4	Yes
7	12	6	Yes	37	8	4	Yes
8	12	6	Yes	38	8	4	Yes
9	12	6	Yes	39	8	4	Yes
10	12	6	Yes	40	8	4	Yes
11	12	6	Yes				
12	12	6	Yes	41	6	4	Yes
13	12	6	Yes	42	6	4	Yes
14	12	6	Yes	43	6	4	Yes
15	12	6	Yes	44	6	4	Yes
16	12	6	Yes	45	6	4	Yes
17	12	6	Yes	46	6	4	Yes
18	12	6	Yes	47	6	4	Yes
19	12	6	Yes	48	6	4	Yes
20	12	6	Yes	49	6	4	Yes
				50	6	4	Yes
21	8	4	Yes	51	6	4	Yes
22	8	4	Yes	52	6	4	Yes
23	8	4	Yes	53	6	4	Yes
24	8	4	Yes	54	6	4	Yes
25	8	4	Yes	55	6	4	Yes
26	8	4	Yes	56	6	4	Yes
27	8	4	Yes	57	6	4	Yes
28	8	4	Yes	58	6	4	Yes
29	8	4	Yes	59	6	4	Yes
30	8	4	Yes	60	6	4	Yes

TABLE IV

GOLD PLATED HOLES TEST NO. 4 (0.016" DIAMETER)

NOTE: Electroless copper plating and electroless nickel plating were each accomplished in 25 minutes.

Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)	Board No.	Electrolytic Copper Plating Time (min.)	Electrolytic Gold Plating Time (min.)	Ten Plated Thru-Holes (Continuity)
1	8	4	Yes	31	6	4	Yes
2	8	4	Yes	32	6	4	Yes
3	8	4	Yes	33	6	4	Yes
4	8	4	Yes	34	6	4	Yes
5	8	4	Yes	35	6	4	Yes
6	8	4	Yes	36	6	4	Yes
7	8	4	Yes	37	6	4	Yes
8	8	4	Yes	38	6	4	Yes
9	8	4	Yes	39	6	4	Yes
10	8	4	Yes	40	6	4	Yes
11	8	4	Yes				
12	8	4	Yes	41	4	2	Yes
13	8	4	Yes	42	4	2	Yes
14	8	4	Yes	43	4	2	No, only 7
15	8	4	Yes	44	4	2	Yes
16	8	4	Yes	45	4	2	No, only 8
17	8	4	Yes	46	4	2	Yes
18	8	4	Yes	47	4	2	No, only 5
19	8	4	Yes	48	4	2	Yes
20	8	4	Yes	49	4	2	Yes
				50	4	2	No, only 6
21	6	4	Yes	51	4	2	Yes
22	6	4	Yes	52	4	2	Yes
23	6	4	Yes	53	4	2	No, only 6
24	6	4	Yes	54	4	2	Yes
25	6	4	Yes	55	4	2	Yes
26	6	4	Yes	56	4	2	No, only 7
27	6	4	Yes	57	4	2	Yes
28	6	4	Yes	58	4	2	No, only 5
29	6	4	Yes	59	4	2	No, only 6
30	6	4	Yes	60	4	2	Yes

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AD- ACCESSION NO.
PP-T-9672-1

Operations Division, Procurement & Production Group, Frankford Arsenal, Philadelphia 37, Pennsylvania

THE PROCESSES AND DEVELOPMENT OF TECHNIQUES OF MINIATURIZED GOLD PLATED THROUGH HOLES IN PRINTED CIRCUITS by Robert P. Hogan and Bernard Stepanski

Report PP-T-9672-1, May 1963, 24 pp incl tables and illustrations UNCLASSIFIED REPORT

This report describes the techniques developed and the procedures used in successfully copper, nickel and gold plating small (0.040", 0.031", 0.020" and 0.016") diameter plated through holes utilised as interface (side-to-side) connections in double sided printed circuit boards.

UNCLASSIFIED

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2. Printed Circuits, Gold Plating Through Holes

I. Hogan, R. P.
II. Stepanski, B.

DISTRIBUTION LIMITATIONS: None; obtain copies from ASTIA

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